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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/771,547	01/30/2001	Toshiyuki Sato	D-1059	8819	
7590 05/18/2006			EXAMINER		
HAUPTMAN KANESAKA BERNER PATNET AGENTS, LLP			AGGARWAL, YOGESH K		
1700 Diagonal I Suite 310	Road	ART UNIT	PAPER NUMBER		
Alexandria, VA	22314	2622			

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	n No.	Applicant(s)					
Office Action Summary		09/771,54	7	SATO ET AL.					
		Examiner		Art Unit					
		Yogesh K.	Aggarwal	2622	:				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SH WHIC - Exter after - If NO - Failu Any I	ORTENED STATUTORY PERIOD FOR RECHEVER IS LONGER, FROM THE MAILING IS IN THE MAILING	NG DATE OF TH FR 1.136(a). In no eve on. period will apply and wil statute, cause the appli	IS COMMUNICATION nt, however, may a reply be tim expire SIX (6) MONTHS from to cation to become ABANDONED	N. nely filed the mailing date of this c D (35 U.S.C. § 133).	,				
Status									
1)[\]	Responsive to communication(s) filed on	27 February 200	96						
2a)□	This action is FINAL . 2b)⊠ This action is non-final.								
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
/	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
4)🖂	4)⊠ Claim(s) <u>1,4,5 and 7</u> is/are pending in the application.								
	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)□	5) Claim(s) is/are allowed.								
	Claim(s) <u>1,4,5 and 7</u> is/are rejected.								
·	Claim(s) is/are objected to.								
8)	8) Claim(s) are subject to restriction and/or election requirement.								
Applicati	on Papers								
9)□	The specification is objected to by the Exa	aminer.							
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.									
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority u	ınder 35 U.S.C. § 119								
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:									
	1. Certified copies of the priority documents have been received.								
	2. Certified copies of the priority documents have been received in Application No								
	3. Copies of the certified copies of the priority documents have been received in this National Stage								
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the continue action pat received.									
* See the attached detailed Office action for a list of the certified copies not received.									
Attachmen									
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date									
3) Inform	r No(s)/Mail Date		5) Notice of Informal Pe		O-152)				

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Response to Arguments

1. In view of the appeal brief filed on 02/27/2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
 - a. (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Ikeda et al. (US Patent # 6,403,965).

 [Claim 1]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figures 2 and 3, element 10) including gate lines (4) and data lines (5) arranged

in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances (2), each being disposed between the pixel electrode and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe (Paragraphs 3, 8 and 10, figures 2 and 3).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of poly-silicon thin film transistors.

However Ikeda teaches an X-ray image detector system wherein the TFTs may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased (col. 12 lines 1-10).

Therefore taking the combined teachings of Applicant's admitted prior art and Ikeda, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10).

[Claim 4]

Applicant's admitted prior art teaches wherein said active matrix board (figure 2: 10) further includes a base plate (figure 2: 11) having high heat resistance and insulating property, an insulating film (figure 2: 2b) disposed on the base plate and sandwiched by the gate lines (figure

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2: 4) and data lines (figure 2: 5), an insulating protecting layer (figure 2: 12) disposed on the insulating film above the switching element, and a common electrode (figure 2: 1b) disposed on the converting layer.

[Claim 7]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figure 3, element 10) including gate lines (4) and data lines (5) arranged in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances (2), each being disposed between the pixel electrode and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation (Paragraph 8), said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300C (Paragraphs 3, 8 and 10, figures 2 and 3).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of poly-silicon thin film transistors.

However Ikeda teaches an X-ray image detector system wherein the TFTs may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased (col. 12 lines 1-10).

Therefore taking the combined teachings of Applicant's admitted prior art and Ikeda, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a

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TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10).

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4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Ikeda et al. (US Patent # 6,403,965) in further view of Yamazaki (US PG-PUB # 2002/0163035).

[Claim 5]

Applicant's admitted prior art teaches a radiation detector-comprising gate driving circuit (figure 3: 6) to be connected to the gate lines (figure 3: 4), a signal driving circuit (figure 3: 7) to be connected to the data lines (figure 3: 5). Applicant's admitted prior art fails to teach a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit. However Yamazaki teaches a signal processing circuits (figure 8: 702 and 703) formed on the active matrix board substrate (figure 8: 100) and connected to the pixel section 701 through gate wiring 704 and source wiring 158 (Paragraph 135). Therefore taking the combined teachings of Applicant's admitted prior art in view of Ikeda it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit as taught in Yamazaki in order to improve the operation performance and the reliability of a semiconductor device by properly using the TFT structures on the same substrate as taught in Yamazaki (Paragraph 19).

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

- 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
- 6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA May 12, 2006

> DAVID OMETZ SUPERVISORY PATENT EXAMINER